Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **Course: B.Tech**

Sub_Code: RCS4C003/RIT4C003

4th Semester Back Examination: 2024-25
SUBJECT: Computer Organization and Architecture
BRANCH(S): CSE, CSEAI, CSEAIML, CSEDS, CST,CSIT, IT
Time: 3 Hours
Max Marks: 100
Q.Code: S499

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) List the functional blocks of a computer and state the role of the control unit.
b) Convert $(-45)_{10}$ into 8-bit 2's complement form.
c) State the difference between fixed-point and floating-point representation.
d) Mention any two characteristics of x86 architecture.
e) Define memory interleaving.
f) Describe the function of the instruction MOV A, M in x86 assembly.
g) Name two types of I/O data transfer techniques.
h) List the three types of pipeline hazards.
i) Differentiate between a program and a process.
j) What is the significance of a write policy in cache memory?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Compare different addressing modes used in instruction set architecture with examples.
b) Illustrate Booth's multiplication algorithm with a suitable example.
c) Differentiate between hardwired and microprogrammed control unit designs.
d) Describe the function and working of the DMA-based data transfer method.
e) Design a ripple carry adder and explain its operation
f) Explain the role of privileged and non-privileged instructions in system control.
g) Draw the instruction execution cycle and annotate each phase briefly.
h) Explain the concept of memory hierarchy with a suitable diagram.
i) Discuss the causes and resolution techniques for cache coherence in multiprocessor systems.
j) Explain the instruction fetch-decode-execute cycle in the context of x86 architecture.
k) Describe the different types of floating-point arithmetic operations with examples.
l) Discuss the benefits and limitations of hyper-threading in modern processors.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four) **(16 x 2)**

Q3	Analyse the instruction set architecture of a basic CPU, including registers, addressing modes, and RTL interpretation. Support your answer with appropriate examples	**(16)**
Q4	Develop a memory module interface for a given CPU organization and illustrate how data is accessed, focusing on semiconductor memory and cache mapping techniques.	**(16)**
Q5	Demonstrate pipeline execution with an example. Evaluate throughput, speedup, and explain how pipeline hazards are managed.	**(16)**
Q6	Design a flowchart to illustrate concurrent memory access and explain cache coherency mechanisms in parallel processors. Extend the discussion to include multi-core scheduling issues.	**(16)**